Analog Layout Engineer

Overview

Position: Analog Layout Engineer
Location: Orange County

Company

Working with an international team you'll be an integral part of a fast-growing company leveraging its strong ultra-high-speed data converters, RF IC, mixed single SOC, and MCM technologies. The role offers impressive growth opportunities in next-generation aerospace and commercial platforms.

Description

.

- A candidate must have working knowledge of high-speed analog layout including detailed transistor level, through the top-level full chip integration, assembly, and full verification and parasitic extraction.

- A candidate must have a clear understanding of layout sensitivities as it pertains to high-speed fully custom analog layout including resistance, capacitance, inductance, RC delay, electro-migration, and cross capacitance.

- Responsibilities include complete physical design:
- Floor Planning – ability to understand the overall goals of the design and visualize the optimal high level physical organization
- Full Custom Layout – including the lowest silicon base transistors layers through the full stack metallization layers.
- Power and Clock Distribution - from the top bump interface to the packaged final product.
- A clear understanding of process flows and how it pertains to high-speed fully custom analog layout performance

- At least three years of experience in CMOS Fin-FET process technologies. Experience in bipolar SiGe process technologies is a plus.

- Candidates should have leadership skills and take ownership of layout deliveries and will provide clear self-generated schedules, work effort estimates, and inform others with clear updates of the design progress.

- Jariet is a small company and positive, cross-discipline relationships are required. Maintaining very close collaboration between design and layout teams is necessary. (We are NOT a “throw the design over the wall to layout” company)

Analog Layout Engineer

Required Skills and Experience

- Experience with high-quality full custom analog layout utilizing the latest Fin-FET\ processes.
- Knowledgeable of layout techniques for device matching, minimizing parasitic, signal shielding, and high-frequency routing.
- Comprehensive understanding of CADENCE layout tools.
- Clear working proficiency of CALIBRE verification tool suite DRC, ERC, LVS, etc., and the ability to interpret the flow output.
- Must have a comprehensive understanding of well-constructed layouts at the transistor base layer level and the ability to work with circuit engineers to drive performance solutions.
- Excellent communication skills are a must, along with a willingness to put oneself forward to drive solutions across diverse teams and functioning groups.
- Scripting skills are a plus.
- US citizenship is required.

Education

- BSEE or equivalent work experience.