Principal Verification Engineer

Overview

Position: Principal Verification Engineer
Reporting to: Verification Manager
Location: Orange County

Company

Jariet is developing breakthrough technologies to permit digital communications technology to be applied at micro/mm-Wave speeds using standard CMOS processes. Jariet is well positioned to provide ASIC products into emerging markets in multi-antenna beamforming communications systems and wireless infrastructure as well as digital deployments into microwave point-to-point links and radar systems. The company provides an exciting work environment with a world class engineering and management team

Job Description

The Design Verification team is growing and has a need for a top talent, senior/principal level, ASIC functional verification engineer. The position may also involve team or project leadership.

Responsible for the development of leading edge verification methodologies for complex high speed digital communication SoCs. Your duties will include, but are not limited to:

- Design and implement verification test bench infrastructure and test cases for system, chip and block level verification, using the latest tools and SystemVerilog class libraries such as OVM, UVM, and VMM.
- Implement Pseudo-random and functional coverage verification methodologies
- Develop functional test and verification plans.
- Work closely with the VLSI Design team to plan and implement design verification strategies.

Required Skills and Experience

- Must be proficient in Pseudo-random and functional coverage verification methodologies
- Strong working knowledge of SystemVerilog and its class libraries such as UVM, OVM or VMM
- SVA, PSL, or OVL assertions
- Formal model checking tools (e.g. Cadence IFV, Jasper) a plus
- Experience with DSP and digital communications a plus
- Good communication skills
- 10+ years' experience and Master's in Electrical Engineering, or equivalent