ASIC Engineer, Physical Design Engineer

Overview

Position: ASIC Engineer, Physical Design
Reporting to: Sr. Director Physical Design
Location: Aliso Viejo, CA

Job Summary

An exciting new fabless semiconductor company seeks an experienced RF Hardware Engineer to develop printed circuit boards for highly integrated monolithic and multi-chip solutions. The position will consist of developing RF The candidate will be involved with the development of new-to-the-world ultra-high speed RF CMOS SOC's and MCM's for a wide range of high frequency commercial, military, and aerospace applications. The person will work with industry leading IC design, package design, and systems engineering experts that are involved in the development of state-of-the-art hybrid digital/RF receivers and transmitters.

Essential Duties

- Develop physical design implementation of multi-hierarchy low-power and high-performance designs, floorplan, place and route, clock tree synthesis, static timing analysis, IR drop, EM, and physical verification in advanced technology nodes.
- Resolve design and flow issues related to the physical design, identify potential solutions, and drive execution.
- Define and implement schemes, including semi-custom placement and routing, to improve performance and power.
- Interface with the RTL design team to drive design modifications to resolve congestion/timing issues and implement functional ECO's.
- Use EDA tool-based programming and scripting techniques to automate and improve throughput and quality.
- Interact with tool vendors to drive tool fixes and flow improvements. Perform tool evaluations of new vendor tools and functions.
- Understanding of scripting languages such as Perl/Tcl, solid understanding of Extraction and STA methodology and tools

Required Skills and Experience

- 5+ years of experience in interpersonal, teamwork, and communication skills and experience interfacing with cross-functional teams, IP, and EDA vendors.
- Experience in physical design and timing closure.
- Experience with EDA tools Innovus/ICC2, Primetime, Redhawk/Voltus, or Calibre.
- Hands-on experience in floor planning, place & route, power and clock distribution, and timing convergence of high-frequency designs.
- Knowledge of static timing analysis and concepts, defining timing constraints and exceptions, corners/voltage definitions.
- **US citizenship required**