Ultra-Low Power 64 GSPS Dual Channel 0.1 - 36 GHz Transceiver with SerDes Baseband Interface

Electra

Features

- ADC & DAC conversion rates from 40 to 64 GSPS
- Operation in 1st Nyquist zone up to 32 GHz
- ADC & DAC directly digitize frequencies through 36 GHz
- Broad instantaneous bandwidth, up to 6.4 GHz
- Scalable decimation and interpolation from 8 to 1024
- Jariet Proprietary digital compensation optimizes spectral purity
- Dual configurable channels enable multiple architectures
- Integrated digital up & down conversion
- API provides user firmware programmability to optimize on-chip direct access to registers
- Selectable internal PLL or externally supplied sample clock provides additional flexibility
- Synchronization inputs as well as direct access to coarse and fine on-chip NCOs well aligned to phased array, MIMO and all applications where data aggregation is desired
- Full duplex, half duplex, and sleep modes supported
- High integration & performance enables elimination of several RF & Microwave analog components from system block diagram, optimizing SWaP-C and thermal generation
- JESD204B/C and JESD204C Serial Data Interface
- Available in a high performance organic BGA package

Applications

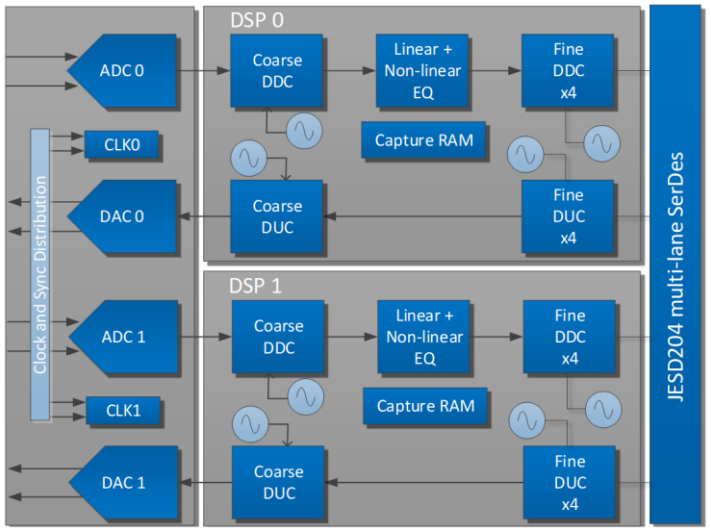
- Military & Aerospace: Radar, EW, EA, ISR, ELINT, Comm
- Commercial: 5G Base Station, PtP, Test & Measurement Equipment, Autonomous Vehicles, Radiometry
- Test and Measurement
- Phased array and data aggregation end uses

General Description

The Electra ASIC is an ultra-high-performance, two channel ADC/DAC transceiver based on Jariet Technologies' ultra-high speed RF data converter technology.

The transceiver enables the end user to eliminate substantial portions of the RF and Microwave block diagram based on the ability to directly digitize waveforms from 40 to 64 GSPS per channel with analog frequencies as high as 36 GHz and instantaneous bandwidths up to 6.4 GHz.

The 10 bit converters are extremely DC power efficient based on state of the art 12 LP CMOS technology, designed and fabricated in the United States at Global Foundries. Each channel is based on interleaved ADCs and DACs followed by programmable digital up and down conversion, linear equalization, decimation and interpolation and a 16-bit SerDes baseband data interface.



Electra Block Diagram

Chip Package

A single fs/16 or fs/32 reference clock is distributed to all channels, and multiplied up by a per-channel PLL to the sample clock. The PLL can also be bypassed and an external fs/2 sample clock applied, to address phase noise sensitive applications.

The ASIC supports full synchronization capabilities, allowing alignment between channels on the ASIC and alignment of channels on multiple ASICs. A synchronization clock at fs/128, fs/256, or fs/512 is required.

Device	Frequency Bands				Max RF (GHz)	f_s (GSPS)	Min Decimation / Interpolation	Max IBW (GHz)	# of Channels	Number of tuners
	UHF, L, S, C, X	Ku	K	Ka						
Electra-MA	✓	✓	✓	✓	36	40 to 64	8	6.4	2	4
Electra-MK	✓	✓	✓		22	40 to 58	16	2.9	2	2
Electra-MX	✓				12	40 to 51.2	32	1.28	2	2